REMARKS

Claims 1-11 are currently pending in the subject application and are presently under consideration. Favorable reconsideration of the subject patent application is respectfully requested in view of the comments herein.

I. Rejection of Claims 1, 2, 6 and 7 Under 35 U.S.C. §102(e)

Claims 1, 2, 6 and 7 stand rejected under 35 U.S.C. §102(e) as being anticipated by Subramanian *et al.* (6,545,753). It is respectfully submitted that this rejection should be withdrawn for at least the following reasons. Subramanian, *et al.* does not teach or disclose the present invention as recited in the subject claims.

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The present invention relates generally to a system and method for detecting voids in an ILD layer. (p. 17, Abstract of the Invention, line 2.) The term "voids" as used in the subject application and understood generally in the art of semiconductor processing is set forth in the Background section of the subject application:

> Undesired fluctuations in any one or a combination of these parameters may lead to void formation in the ILD. In many current applications, ILD formation must conform to exacting specifications in order to mitigate or prevent void formation. A void present in the ILD may cause electrical shorting (short circuits), cracking in the circuit, and/or lead to an open circuit depending on the size and location of the void. For example, voids which exceed about 25% of a structure width and/or are higher than the structure surface in height tend to cause any one or a combination of these problems. Voids which are formed early on in the semiconductor fabrication process but are undetected until further processing has been done may exacerbate or cause even more problems, resulting in an inoperable device.

> With the requirement of smaller and smaller features and higher device densities, detection and mitigation of void formation is even more critical to the fabrication of operable and effective semiconductor devices. Thus, to detect the formation of voids, including their size and number, an efficient system/method to monitor ILD deposition for void formation and detection is desired to increase the reliability and performance of semiconductor devices.

(p. 1, line 30 – p. 2, line 12, emphasis added.)

Independent claim 1 is directed to a "system for detecting and monitoring ILD void formation comprising ... a processor operatively coupled to the measuring system, the processing receiving ILD parameter data from the measuring system and the processor using the data to determine the present of a void in the ILD layer." (emphasis added.)

To the contrary, Subramanian *et al.* is directed to "a system for monitoring and/or controlling an etch process associated with a dual damascene process *via* scatterometry based processing..." (Abstract). Further, "[l]ight reflected from the features and/or grating is collected by a measuring system which processes the collected light. The collected light is indicative of the etch results achieved at respective portions of the wafer. The measuring system provides etching related data to a process that determines the desirability of the etching of the respective portions of the wafer. ... The processor produces a real time feed forward information to control the etch process, in particular, terminating the etch process when desired end points have been encountered." (Abstract).

The Examiner contends that "the interconnecting holes [of Subramanian *et al.*] are equivalent to the voids claimed in the limitations." (Office Action at p. 3.) Applicants' representative respectfully submits that the Examiner's position is incorrect. As discussed above, the presence of "voids" in a semiconductor are generally not desirable; for example, "[t]he processor selectively marks the ILD layer portions to facilitate further processing and/or destruction of the IC with the ILD layer voids." (p. 17, Abstract, lines 8-10.) To the contrary, the "interconnecting holes" produced by the system and/or method of Subramanian *et al.* are functional elements of semiconductor(s); for example, "[t]he precision with which resist portions are removed to create vias and interconnecting

holes and the resulting precision in the distance between the remaining portions corresponds to the precision with which desired profiles, depths, CDs, *etc.* are achieved." (Col. 7, lines 19-23.)

Thus, it is respectfully submitted that Subramanian *et al.* does not teach or disclose the limitation of the processor using the data to determine the presence of a void in the ILD layer. Accordingly, it is respectfully submitted that independent claim 1, and, claims 2, 6, 7 which depend therefrom, are allowable. Withdrawal of this rejection is respectfully requested.

II. Rejection of Claims 3-5 Under 35 U.S.C. § 103(a)

Claims 3-5 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Subramanian *et al.* ('753) as applied to claim 3 above, and further in view of Kleinknecht *et al.* (4,330,213). It is respectfully submitted that this rejection should be withdrawn for at least the following reasons.

Subramanian *et al.* does not qualify as prior art against the subject application since the subject matter of Subramanian *et al.* and the claimed invention, at the time the invention was made, was subject to an obligation of assignment to Advanced Micro Devices, Inc. Accordingly, this rejection should be withdrawn.

Moreover, the combination of Subramanian *et al.* and Kleinknecht *et al.* does not make obvious the subject invention as recited in claims 3-5.

The references if combined as suggested by the Examiner would not result in the invention as claimed.

> It is essential to consider all elements of the claimed invention; it is impermissible to compare the prior art with what the viewer interprets the "gist" of the invention to be *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 19 USPQ2d 1111 (Fed. Cir. 1991); *Perkin-Elmer Corp. v. Computervision Corp.*, 732 F.2d 888, 221 USPQ 669 (Fed. Cir. 1984); *Jones v. Hardy*, 727 F.2d 1524, 1527-28, 220 USPQ 1021m 1024 (Fed. Cir. 1984).

As discussed previously, Subramanian *et al.* does not teach or disclose the limitation of the processor using the data to determine the presence of a void in the ILD layer recited independent claim 1. Claim 5 is dependent upon claim 4 which is dependent upon claim 3, which depends from independent claim 1. The combination of Subramanian *et al.* with Kleinknecht *et al.* does not result in the subject invention as the limitation of the processor using the data to determine the presence of a void in the ILD layer recited in independent claim 1 is not taught, suggested or disclosed. As claims 3-5 depend from independent claim 1, it is respectfully submitted that claims 3-5, are allowable. Withdrawal of this rejection is respectfully requested.

III. Rejection of Claims 8-11 Under 35 U.S.C. § 102(e)

Claims 8-11 stand rejected under 35 U.S.C. §102(e) as being anticipated by Subramanian *et al.* (6,545,753). It is respectfully submitted that this rejection should be withdrawn for at least the following reasons.

As noted previously, applicants' representative respectfully submits that the Examiner's position with regard to the interconnecting holes of Subramanian *et al.* being equivalent to the voids of the subject application is incorrect.

Independent claims 8 and 10 recite a limitation of "comparing a reflected light array from the at least one portion to a database, where the database comprises known ILD layers having at least one void present, to determine the presence of the at least one void in the at least one portion associated with the ILD layer". (Emphasis added). As discussed previously, Subramanian *et al.* is directed to "a system for monitoring and/or controlling an etch process associated with a dual damascene process *via* scatterometry based processing..." (Abstract). Subramanian *et al.* does not teach or disclose the limitation of comparison to determine the presence of void(s) in at least one portion associated with the ILD layer.

Further, independent claims 8 and 10 further recite a limitation of "selectively marking the ILD layer grid block as having the at least one void". Subramanian *et al.* does not teach or disclose this limitation.

Finally, independent claim 11 recites a limitation of "means for detecting ILD void formation in a plurality of portions of the ILD layer". For the reasons stated previously with regard to detection of voids, applicants' representative respectfully submits that Subramanian *et al.* does not teach or disclose this limitation.

Accordingly, it is respectfully submitted that independent claims 8, 10 and 11 (and claim 9 which depends from claim 8) are allowable. Withdrawal of this rejection is respectfully requested.

CONCLUSION

The present application is believed to be in condition for allowance in view of the above comments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 (Reference AMDP595US).

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

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